Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] [c1]

A memory system comprising:
a plurality of DRAMs having circuits to accept non-inverted input signals and inverted input signals.
a register programmed to provide inverted or non-inverted signals to the DRAMS.

[c2] [c2]

The memory system of claim 1 which includes re-drive circuitry, which can output both non-inverted and inverted polarity signals from one or more input signals.

[c3] [c3]

A memory system according to claim 1 which includes:
Programmable pins in the register and DRAMs to operate in either non-inverted or inverted mode.

[c4] [c4]

A memory system according to claim 3 wherein the DRAMs are mounted on a DIMM.

[c5] [c5]

The memory system of claim 3 wherein one programmable pin is connected to ground to provide one

mode and the other programmable pin is connected to Vdd to operate in the other mode.

[c6] [c6]

A memory system comprising:

a plurality of DRAMs having circuits to accept non-inverted input signals and inverted input signals; and

a memory controller which can drive either non-inverted or inverted signals to the DRAMs using a programmable pin.

[c7] [c7]

A memory system according to claim 6 wherein the memory controller may operate in one mode at powerup and a means for changing modes after powerup.

[c8] [c8]

The memory system of claim 6 wherein the pin is hard-wired to the DRAMs.

[c9] [c9]

A memory system of claim 1 in which the register drives either non-inverted or inverted signals to the DRAMs using a programmable pin.

[c10] [c10]

A memory system comprising:

a module having a plurality of DRAMs with inputs and

outputs and circuits to accept either non-inverted input signals and inverted input signals;
a means connected to the circuits for changing modes to accept inverted input signals; and
a memory controller which is programmable to operate in non-inverted mode at power up and to change after it is programmed.

[c11] [c11]
A memory system of claim 10 wherein pre-selected DRAMs may operate in the inverted mode with some critical signals remaining in a non-inverted mode.

[c12] [c12]
The memory system of claim 10 wherein the memory controller may operate in the inverted mode with some critical signals remaining in non-inverted mode.

[c13] [c13]
The memory system of claim 10 wherein a programmable pin is hard-wired to the module.

[c14] [c14]
The memory system of claim 10 wherein the means for changing modes includes a pin that is controlled by the memory controller.

[c15] [c15]

A DIMM comprising:

a plurality of DRAMs with means for operating with non-inverted or inverted signals based on a pre-selected operating mode; and

signal re-drive circuitry which generates an output in both non-inverted and inverted polarity signals from one or more input signals.

[c16] [c16]

A computer system with a memory system comprising: memory devices and re-drive circuitry external to the said memory devices, said re-drive circuitry having means for outputting both non-inverted and inverted polarity signals from one or more input signals, and said memory devices designed to operate with non-inverted or inverted signals based on a selected operating mode.